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EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/780,054	PARRUCK ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 6-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28* is/are allowed.

6)☒ Claim(s) *1,6-23,26 and 27* is/are rejected.

7)☒ Claim(s) *24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1 and 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gun (USP 5777984) in view of Caldara (USP 5748629), Yin (USP 6219728) and McClure (USP 5790770).

Regarding claims 1 and 7-16, Gun discloses a data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including a switch element having a switch matrix (Fig 5, Ref 154); at least one input switch access port structure coupled to said switch matrix containing a plurality of input back pressure buffer

structures wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis (Figs 6-7, Ref 141 and Fig 5 or 8, Ref 140 which includes a plurality of per VC queue and feedback for generating a feedback signal to the source that is transmitting the data cell to the switch 154); a plurality of input ports (Fig 5, Ref 160) coupled to said at least one input switch access port structure (Fig 5, Ref 140) wherein said plurality of input ports are coupled to a plurality of traffic generators (Fig 4, Ref 102); a size of said plurality of input back pressure buffer structures are individually set (Fig 8, Ref 290); a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure (Local Threshold is maximum and minimum is zero; See col. 11, lines 5-67); a size of said plurality of input back pressure buffer structures is configured for a plurality of said virtual connections (col. 11, lines 5-67 and Fig 8, Ref 290). However, Gun fails to disclose at least one output arbitration structure coupled to said switch matrix and coupled to said plurality of output ports wherein said at least one output arbitration device represents the circuitry for arbitrating access to a single output port of said plurality of output ports and a switch includes a plurality of buffer structures being configured to allow buffering to be accomplished on a per virtual connection basis and an input backpressure between the switches based on per VC. In the same field of endeavor, Caldara discloses a switch comprising at least one output arbitration structure (Fig 1, Ref 12) coupled to said switch matrix (Fig 1, Ref 13) and coupled to said plurality of output ports (Fig 1, Ref 22) wherein said at least one output arbitration device (Fig 1, Ref 13) represents the circuitry for arbitrating access to a single output port of said plurality of output ports; and a plurality output

ports coupled to said output arbitration portion wherein said pluralities of output ports are coupled to a plurality of output destinations (Col. 4, lines 60 to col. 5, lines 42); each output arbitration structure of said at least one output arbitration structure includes a plurality of schedulers and a plurality of selectors (Fig 6, Ref VBR, ABR and UBR schedulers has a first selector for selecting one of the schedulers and scheduler for preferred list wherein the selector are coupled to the first selector and second selector for outputting the cell onto the link); each scheduler of said plurality of schedulers is configured to schedule ATM cells on one of a per-virtual connection basis, a per-port basis, a per traffic class, a per priority basis, a per group of virtual connections basis, and a cells similarly grouped basis (Fig 6, Ref VBR, ABR and UBR schedulers; arbitration is performed on a per virtual connection basis wherein said each scheduler of said plurality of schedulers are coupled to connections having a same priority for switching (Fig 6, Ref VBR, ABR and UBR schedulers based on priority such as ABR, VBR and UBR); each scheduler of said plurality of schedulers is coupled to at least two buffer structures having a same priority (Fig 6, Ref VBR, ABR and UBR schedulers wherein the queues store the same priority cell such as ABR, VBR and UBR); each selector of said plurality of selectors is configured to select ATM cells using at least one of a round-robin selection technique and a weighted round-robin technique and said at least one output arbitration structure includes one of said plurality of selectors for every ATM output (col. 13, lines 46-52). However, Gun and Caldara fail to disclose an input backpressure between the switches and switch includes a plurality of buffers for storing the packets based on Per VC. In the same field of endeavor, McClure discloses a switch comprising a switch fabric and plurality of input and out port, wherein each contains a queue which includes a plurality of per VC queues (Col. 2, lines 10-46,

col. 4, lines 44-60 and col. 6, lines 10-20) and plurality of input back pressure buffer structures are configured for said plurality of virtual connections having a same priority (Col. 6, lines 10-20). However, Gun, McClure and Caldara fail to disclose a switch includes a plurality of buffers for storing the packets based on Per VC. In the same field of endeavor, Yin discloses a switch includes a plurality of buffer structure for storing the packets based on Per VC (Col. 10, lines 41-46 and Fig 2, and 5-7).

Since, Gun suggests feedback method at the input queue and Caldara suggests a method and system for feedback between the input and output buffer and McClure suggests the use of input feedback for per VC in a nest of queues of queues. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a shared buffer in the switch which used to store the data packet based on per VC as disclosed by Yin into a feedback at input per queue as disclosed by McClure's method and system into Caldara's method and system which discloses a arbitration structure comprising a plurality of schedulers and selectors into the method and system of Gun. The motivation would have been to prevent a data loss and improve the throughput of the system.

Regarding claims 17-20, Gun discloses (Figs 1-15 and col. 1, line 15 to col. 24, line 14) a data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including a switch element having a switch matrix (Fig 5, Ref 154); at least one input switch access port structure coupled to said switch matrix containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer

structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis (Figs 6-7, Ref 141 and Fig 5 or 8, Ref 140 which includes a plurality of per VC queue and feedback for generating a feedback signal to the source that is transmitting the data cell to the switch 154); a plurality of input ports coupled to said at least one input switch access port structure, wherein said plurality of input ports are coupled to a plurality of traffic generators (Fig 5, Ref 141 are coupled to the Ref 160 for receiving data from the sources); and at least one output switch access structure coupled to said switch matrix, and at least one output port coupled to said at least one output switch access structure, wherein said at least one output port is coupled to a plurality of output destinations (Fig 5, Ref 142 for coupling to the switch and the output ports which couples to the destination); a size of said plurality of input back pressure buffer structures are individually set (Fig 8, Ref 290); a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure (Local Threshold is maximum and minimum is zero; See col. 11, lines 5-67). However, Gun fails to disclose said at least one output switch access structure including, a plurality of schedulers, an at least one selector, an at least one switch matrix output port; arbitrates access to a respective said at least one output port and a switch includes a plurality of buffer structures being configured to allow buffering to be accomplished on a per virtual connection basis and an input backpressure between the switches on per vc. In the same field of endeavor, Caldara discloses at least one output switch access structure (Fig 1, Ref 22) including, a plurality of output queues for storing the packets based on per VC (Col. 5, lines 30-42); arbitrates access to a respective said at least one output port (Fig 1, Ref 12 has an output port to

the switch and selecting a output port for transferring the data from the input to the output ports) and the output port includes a plurality of buffers wherein each buffer for storing the packets of a VC (Fig 2, Ref 34 and col. 2, lines 17-43 wherein the input and output queues are per VC pair). However, Gun and Caldara fails to disclose an input back pressure between the switches based on per vc and switch includes a plurality of buffer structures being configured to allow buffering to be accomplished on a per virtual connection basis. In the same field of endeavor, McClure discloses a switch comprising a switch fabric and plurality of input and out port, wherein each contains a queue which includes a plurality of per VC queues (Col. 2, lines 10-46, col. 4, lines 44-60 and col. 6, lines 10-20) and plurality of input back pressure buffer structures are configured for said plurality of virtual connections having a same priority (Col. 6, lines 10-20) and output port includes the per VC buffer for storing the packets of a VC (Col. 2, lines 10-46). However, Gun, McClure and Caldara fail to disclose a switch includes a plurality of buffers for storing the packets based on Per VC. In the same field of endeavor, Yin discloses a switch includes a plurality of buffer structure for storing the packets based on Per VC (Col. 10, lines 41-46 and Fig 2, and 5-7).

Since, Gun suggests feedback method at the input queue and Caldara suggests a method and system for feedback between the input and output buffer and McClure suggests the use of input feedback for per VC in a nest of queues of queues. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a shared buffer in the switch which used to store the data packet based on per VC as disclosed by Yin into a feedback at input per queue as disclosed by McClure's method and system into Caldara's method and system which discloses an output buffers are configured for storing the packets based on per

VC into the method and system of Gun. The motivation would have been to prevent a data loss and improve the throughput of the system.

4. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gun, McClure, Yin and Caldara as applied to claim 17 above, and further in view of Chiussi (USP 5689500).

Regarding claim 21, Gun, McClure and Caldara fail to discloses said at least one output arbitration device schedules cells inputted into said input ports in accordance to a weight accorded to each cell of said plurality of cells. In the same field of endeavor, Chiussi discloses a packet scheduler for scheduling the packets based on the weight (col. 12, lines 32-39).

Since, Gun, McClure and Caldara suggest the enqueued cell must be scheduled to transfer onto an output link and Caldara suggests round robin scheduling method. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a weight round robin as disclosed by Chiussi's method and system into the system and method of Gun, McClure and Caldara. The motivation would have been to improve the throughput of the system.

5. Claims 22-23 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuboi (USP 5140582).

Regarding claims 22 and 26-27, Tsuboi discloses (Figs 1-37 and col. 1, lines 5 to col. 38, lines 28) switch element (Fig 3) comprising an input routing portion including a switch matrix input port for receiving data (Fig 3, Ref 21) from traffic generators (Fig 22, Ref 505); a buffer portion including a plurality of buffers (Fig 3, Ref 121 and 122); a switch matrix portion for routing data out from the plurality of buffers (Fig 3, the link between the buffers 121-122 and the schedulers 1411-1412 and 1421-1422); a plurality of schedulers for receiving the data from the

plurality of buffers through the switch matrix (Fig 3, Ref 1411-1412 and 1421-1422 are the schedulers for receiving the data from the buffers via the links between them "read on switch matrix"); a selector (Fig 3, Ref 181 for receiving a data from the schedulers "1411 and 1412" and outputting packet to an output port) for receiving data from the plurality of schedulers, the selector enabling output from the switch element through a switch matrix output port to a traffic acceptors (Fig 2, Ref 505). However, Tsuboi fails to disclose the schedulers receive data via a switch matrix. Since, Tsuboi suggests a crosspoint. However, in the same field of endeavor, it would have been obvious to one of ordinary skill in the art to apply a switch for establishing a link between the input and output ports into the links between buffers and schedulers. The motivation would have been to reduce the cost of the system.

Regarding claim 23, Tsuboi discloses an additional input routing portion including an additional switch matrix input port for receiving data; an additional buffer portion including an additional plurality of buffers, the switch matrix portion routing data out from the additional plurality of buffers; an additional output arbitrating portion, including an additional plurality of schedulers for receiving the data from the additional plurality of buffers through the additional switch matrix, and an additional selector for receiving data from the additional plurality of schedulers, the additional selector enabling output from the switch element through an additional switch matrix output port (Fig 2 discloses the packet switching system comprise a plurality of 21-2n and Fig 4 discloses additional of the input routing portion, buffers, schedulers, selector, switch matrix). However, Tsuboi fails to disclose the schedulers receive data via a switch matrix. Since, Tsuboi suggests a crosspoint however, in the same field of endeavor, it would have been obvious to one of ordinary skill in the art to apply a switch for establishing a link between the

input and output ports into the links between buffers and schedulers. The motivation would have been to reduce the cost of the system.

Allowable Subject Matter

6. Claim 28 allowed.

7. Claims 24-25 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As claims 24-25 and 28, the prior arts fail to disclose a switch element, comprising: a first input routing portion including a first switch matrix input port for receiving data; a first buffer portion including a first plurality of buffers; a switch matrix portion for routing data out from the first plurality of buffers and a second plurality of buffers; a first output arbitrating portion, including, a first plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix, a first selector for receiving data from the first plurality of schedulers, the first selector enabling output from the switch element through a first switch matrix output port; a second input routing portion including a second switch matrix input port for receiving data; a second buffer portion including the second plurality of buffers; a second output arbitrating portion, including, a second plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix, a second selector for receiving data from the second plurality of schedulers, the second selector enabling output from the switch element through a second switch matrix output port; a plurality of traffic generators for inputting data into the first input routing portion .

and the second input routing portion; and a plurality of traffic acceptors to receive data from the first output arbitrating portion and the second output arbitrating portion.

Response to Arguments

8. Applicant's arguments filed 3/24/05 have been fully considered but they are not persuasive.

In response pages 11-12, the applicant states that Gun fails to disclose input switch access port having input backpressure for per VC queues. In reply, Gun discloses an input port structure which comprising a plurality of per VC queues wherein each per VC queue includes a input backpressure so that when the per VC queue is overloaded, it generates a feedback message "BRM" to notify the source which are transmitting the packets to the per VC queue to stop transmitting (Col. 11, lines 6-67, See Fig 5, Ref 140 and 160 are input port structure and 146 and 162 are output port structure).

In response to pages 12-13, the applicant states that the applicant claims do not require some of the feature of Caldara such dynamic allocation of bandwidth by the bandwidth arbiter to look for open port from FSPP for assigning the packet to TSPP. In reply, the teaching of Caldara is performed the claimed invention because the claims does not excludes those features of the Caldara structure.

In response to pages 13-14, the applicant states that McClure does not disclose input backpressure for per VC and output port includes a queue for each per VC. In reply, McClure discloses a switch with includes a plurality of input and output buffers wherein each input or output buffer is divided into a plurality of queues wherein each queue stores the cells having a

same VC (Fig 2, col. 6, lines 10-20) and the input per VC queue of the second node generates a feedback message to the output per VC queue of the first node (Col. 2, lines 10-25 and Fig 3 which discloses a structure and method for generating a feedback message from the input queues of the node 12 to the node 12a in order to perform a flow control based on a virtual connection).

The teaching of the references discloses the features of the claims.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to page 15, the applicant states that Tsuboi does not disclose (1) a plurality of schedulers that receiving the packets from the buffers through the switch; (2) does not suggest replacing a bus with a switch. In reply, Tsuboi discloses with respect to (1) a plurality of schedulers (Fig 3, Ref 1411-1412 and 1421-1422) that receiving the packets from the buffers (Fig 3, Ref 121 and 122) through the links between them (read on switch); with respect to (2), the use of switch matrix is well documented in the art of switching because of its advantages, such as to provide a fixed, uniform, unpredictable path independent time delay for all signals that passed through the switch matrix (USP 5015884, See Abstract); or to provide enhanced signal availability and routability (USP 5617042, See abstract) or easily to expand the network (USP 5612953) and replacing a bus with a switch (USP 5822319, See col. 25, lines 42-50). Thus, the motivation of using switch matrix in the system of Tsuboi would have been to provide a fixed, uniform, unpredictable path independent time delay for all passing signals. Futhermore, Tsuboi discloses claim 23 requires an additional exact configuration of claimed invention in claim 22.

Although, figure 3 shows a 2x2 system with two inputs and two outputs, in figure 4 Tsuboi suggests that the system can be expanded using multiple system of figure 3 to accommodate more inputs and outputs. Since Tsuboi suggest the expansion, official notice is now needed in rejecting claim 23. Motivation to expand/multiply the system of figure 3 should have been to enhance system capacity to accommodate more inputs and outputs and claim 27 requires traffic acceptors to receive data form the output of the switch element. These traffic acceptors are terminals/stations/nodes that communicate with the switch element. In Tsuboi's system, these terminals 505 (traffic acceptors) shown in figure 22 communicate with the switch (left portion of figure 22).

The teaching of Tsuboi discloses the claimed invention.

Conclusion

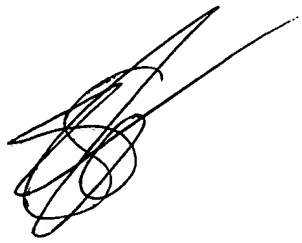
9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven HD Nguyen
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6/25/05